B. V. V. Sangha's
Basaveshwar Engineering College (Autonomous), Bagalkot
Department of Electronics and Communication Engineering

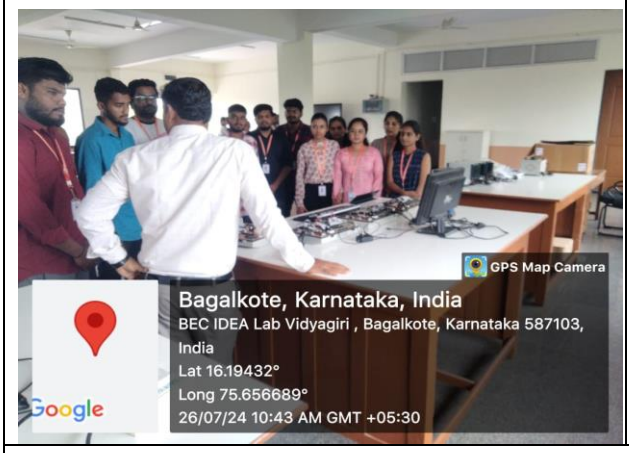
Best Practices in The Department

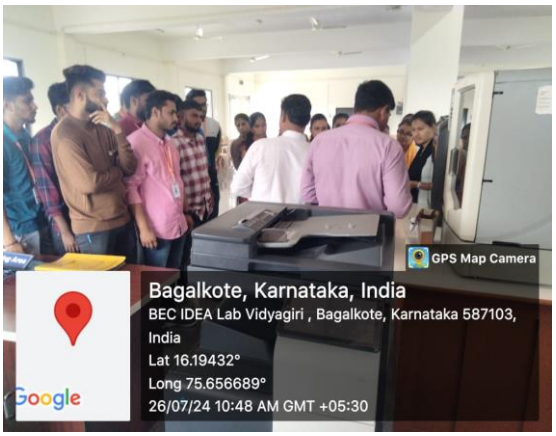
Sl.No.	Best Practices Adapted	Date/Year	Report With Photographs (Link) (Optional)
1.	The department is having a club called **Software Coding Club.** It is formed to enhance the software skills of the students. Software skills are the need of the hour for our students. It is coordinated by faculty of the department. Various software coding competitions are arranged for the students in which students of other department also participate. The competitions are of industry level so that students become confident in facing placement tests and other competitive examinations. Every semester software coding competitions are being organized.	**2020**	
2.	The department is having a club called VLSI **Club.** It is formed to enhance the knowledge of digital electronics, electronic circuits and VLSI subjects of the students. Knowledge in the area of digital electronics, electronic circuits and VLSI are the need of the hour for ECE students. It is coordinated by faculty of the department. Various circuit building and circuit debugging competitions are arranged for the students in which students of other allied departments also participate. The competitions are of industry level so that students become confident in facing placement tests and other competitive examinations. Every semester circuit building, circuit debugging and VLSI related competitions are being organized for the benefit of students.	**2020**	

3.	Think, pair, share activity for first year students This activity helps to monitor and support students to work together through the following process: T : (Think) Teachers begin by asking a specific question about the text. Students "think" about what they know or have learned about the topic. P : (Pair) Each student should be paired with another student or a small group. S : (Share) Students share their thinking with their partner. Teachers expand the "share" into a whole-class discussion Subject: Basic Electronics Sem: I Topic: Types of Oscillators	**2020**	

Photographs showing students visit to IDEA lab, Radio station, SCADA lab and BOSCH lab

1). Idea Lab





Idea Lab visit by ECE department students

2). Radio Station

Radio station visit by ECE department students

3). SCADA Lab

SCADA lab visit by ECE department students

4). BOSCH Lab

BOSCH lab visit by ECE department students

ICT Tools Usage

Sl No	Course Name	ICT tool used
1.	Digital Signal Processing	PPT
2.	Microwave and Antennas	PPT
3.	CMOS digital system design	PPT and youtube video for visualization https://youtu.be/3XTWXRj24GM?si=RSqPLKAYJkebD1gx

Course Projects

Academic Year: 2023-24

Course name: Analog Circuit Design Subject code: 22UEC403C

The projects listed in the document are:

1. **Turn On and Turn Off Switch Using 555 Timer**
2. **Metal Detector Using 555 Timer IC**
3. **Sound Detector Using 555 Timer IC**
4. **Automatic Light Fence Circuit with Alarm**
5. **Temperature Sensor Using LM35**

Guide

Dr. Mamata Sataraddi

B.V.V.S
BASAVESHWAR ENGINEERING COLLEGE, BAGALKOTE
DEPARTMENT: ELECTRONICS AND COMMUNICATION ENGINEERING
ACADEMIC YEAR: --2023-24 (V SEMESTER)

Course projects

Sub: CMOS Digital VLSI Design **Sub code: 21UEC503C**

Faculty: Dr. Sarojini B. K.

Sl. No.	Name of the course Project	Student R. Nos.
1.	Design and simulate 4:1 MUX using 2:1 MUX, and 2:1 MUX should be designed using transmission gates.	1, 2, 3, 4, 5
2.	Design and simulate full adder using logic gates.	6, 7, 8, 9, 10,
3.	Design and simulate positive level sensitive D latch.	11, 12, 13, 14, 15
4.	Design and simulate negative level sensitive D latch.	16, 17, 18, 19, 20
5.	Design and simulate 4 bit parallel adder using full adders.	21, 22, 23, 24, 25
6.	Design and simulate positive edge triggered flip flop in CMOS	26, 27, 28, 29, 30
7.	Design and simulate full adder using PLA.	31, 32, 33, 34, 35
8.	Design and simulate negative edge triggered flip flop in CMOS.	36, 37, 38, 39, 40
9.	Design and simulate 4:1 MUX using tristate inverters.	41, 42, 43, 44, 45
10.	Design the CMOS circuit and simulate the Boolean expression Q = AB + CDE by incorporating the logic into latches.	46, 47, 48, 49, 50

SUBJECT: DSD using Verilog (21UEC506E)
Div:5th B
Staff incharge: M. C. Aralimarad
DSD using Verilog Assignment Project List B division 2023-24

Sl.No	Student Name of Project	USNs	Name of Project
1.	Samiksha J P Prerana K P	2BA21EC083 2BA21EC069	Dual Port Ram with its testbench
2.	Swati I Bangari Sushma V Aski	2BA21EC115 2BA21EC113	Door locking system with its testbench
3.	Shivprakash Math Rahul Kulkarni	2BA21EC094 2BA21EC071	ROM with its testbench
4.	Sneha karoli Sachin kurubagatti	2BA22EC410 2BA21EC081	N Bit multiplier
5.	Darini R Budihal	2BA21EC029	4-bit Parallel adder using for loop
6.	Aishwarya. Hiremath Pavitra S Patil	2BA21EC007 2BA21EC053	Fibonacci series With its testbench
7.	Pankaj D.Gunjikar Varsha R.Mugati	2BA21EC051 2BA21EC118	Serial peripheral interphase
8.	Akshata D Bhagyashree B	2BA21EC012 2BA21EC027	finding A Square root using counter with testbench
9.	Shivali Hiremath Priyanka Nidagundi	2BA21EC128 2BA22EC407	PWM Shift register
10.	Shreenidhi K Vivek L	2BA21EC095 2BA21EC126	ELEVATOR OPERATION
11.	Siddanagowda P Sunil G	2BA21EC099 2BA21EC111	WASHING MACHINE OPERATION
12.	Prasannakumar Patil Shashidhar Nandi	2BA21EC061 2BA21EC091	Ring Counter
13.	Naveen s.k N Vallabh	2BA21EC046 2BA21EC044	Binary to gray & its vice-versa with its testbench code
14.	Megha c shirol Priya M Malaghan	2BA21EC042 2BA21EC070	Traffic Light Controller
15.	Preksha betala Soumyashri Teradal	2BA21EC068 2BA21EC105	Stop watch
16.	Shashank N maradimath	2BA22EC408 2BA21EC129	smart_attendance_system
17.	Basuraj I Bisaguppi Rakesh Desai	2BA21EC026 2BA21EC072	Device selector using MUX

18	Preetam Kanal Pratham Asuti	2BA21EC067 2BA21EC063	8:1 DEMUX
19	Suhas R Hatti	2BA21EC108	Bubble Sort With Test Bench
20	Appuraj R K Ranganath P	2BA21EC018 2BA21EC076	Voting Machine Operation
21	Diya Mantri Shaila Dalawai	2BA21EC030 2BA21EC089	32 Bit Adder
22	Vijayalaxmi Bagewadi Kavya kuntargi	2BA21EC123 2BA22EC403	Clock Divider

DSD using Verilog Assignment Project List A division 2023-24

Sl.No	Student Name of Project	USNs	Name of Project
01	Suyog A Shinde Achyut Hipparagi	2BA21EC114 2BA21EC004	Newspaper Vending Machine
02	Vinay Basava Prajwal Desai	2BA21EC124 2BA21EC057	Two's complement fixed point arithmetic
03	Snehashri A Ambore Aishwarya Gurav	2BA21EC101 2BA21EC006	Automative RADAR Signal detector
04	Saraswati Gosabal Soujanya Kanthi	2BA21EC087 2BA21EC103	UART Receiver
05	Veeresh Soodi Pankaj Biradar	2BA21EC121 2BA21EC050	Clock with Alarm
07	Pavan Kumatole Praveen Hatti	2BA21EC052 2BA21EC065	Ripple Counter
08	Anjaney M Desai Arun Budni	2BA21EC017 2BA21EC020	Wallace Tree Multiplier.
09	Pallavi B H Pratiksha M D	2BA21EC049 2BA21EC069	4:1 Mux using sequential circuit.
10	Aditi Shah Akshata Desai	2BA21EC005 2BA21EC013	Armstrong number with it's test bench
11	Rohit kumbarhall Kartik patil	2BA21EC080 2BA21EC036	Temperature controller

12	Pragati P Laxmi N	2BA21EC055 2BA21EC040	Full adder using two half adder
13	Gagan B Basavaraj urf Koushik	2BA21EC031 2BA21EC025	FIFO Memory
14	Aishwarya Mantrannavar Varshita J	2BA21EC007 2BA21EC119	Conversion of Octal to Binary and addition of them
15	Amruta K Rekha G	2BA21EC015 2BA21EC078	Conversion of Binary to Hexadecimal and addition of them
16	Rakshita G Suchitra H	2BA21EC075 2BA21EC107	Full subtractor using two half subtractors
17	Narayan N Malabasari Kiran Muradi	2BA21EC045 2BA21EC038	Hexadecimal keypad scanner
18	Soumya. K Aishwarya.H	2BA21EC104 2BA21EC009	Car parking system
19	shahil Ismail tankasali Nitish	2BA21EC088 2BA21EC048	Sequence detector
20	Abhishek Anand S H	2BA21EC002 2BA21EC016	Implementation of double ended queue
21	Prajwal H K Avinash	2BA21EC058 2BA21EC023	Waste segregation at home
24	Arundati V.B Rakshita R.J	2BA21EC021 2BA21EC073	Johnson counter using d-flipflop
25	Siddhant M Magadum Shrinidhi Joshi	2BA21EC100 2BA21EC096	Audio Mixer with its test bench
26	Srivatsa Avadhani Karthik Kulkarni	2BA21EC106 2BA21EC037	Robotic arm controller with its test bench
27	Abhinandan samay MohammadRehan R Pattankudi	2BA21EC001 2BA21EC043	Substraction using 2's complement
28	Shivananda Chandrashekhar G Hadalagi	2BA21EC093 2BA21EC028	D-flipflop using transmission gates
29	Sangamesh Kuppast Basavaraj Metagudda	2BA21EC085 2BA22EC401	4-bit parallel adder using generate statement