# V Semester

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<th>Subject Code</th>
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<td>1</td>
<td>UEC511C</td>
<td>Digital Signal Processing</td>
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<td>UEC512C</td>
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<td>3</td>
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<td>Circuit Design with VHDL</td>
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<td>7</td>
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<td>DSP and VHDL Lab</td>
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### Elective-I

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<td>Pulse and Switching Circuits</td>
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<td>3</td>
<td>UEC520E</td>
<td>Data Structures using “C”</td>
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Unit I

Discrete Fourier Transforms (DFT): Frequency domain sampling and reconstruction of discrete time signals. DFT as a linear transformation, its relationship with other transforms, properties, multiplication of two DFTs, the circular convolution, additional DFT properties, use of DFT in linear filtering, overlap-save and overlap-add method.

Unit II

Fast-Fourier-Transform (FFT) algorithms: Direct computation of DFT, need for efficient computation of the DFT (i.e. FFT algorithms). Radix-2 FFT algorithm for the computation of DFT and IDFT, decimation-in-time and decimation-in-frequency algorithms. Goertzel algorithm, and chirp-z transform algorithm.

Unit III

IIR filter design: Characteristics of commonly used analog filters – Butterworth and Chebyshev filters. Design of IIR filters from analog filters (i.e. Butterworth and Chebyshev) impulse invariance method, and approximation of derivative (backward difference, forward difference and bilinear transformation) method.

Unit IV

FIR filter design: Introduction to FIR filters, spectrum of various windows used in FIR filter design, design of FIR filters using windowing (Rectangular, Hamming, Hanning and Bartlet) method. FIR filter design using frequency-sampling method. Implementation of discrete-time systems: Structures for IIR and FIR systems-direct form I and direct form II systems, cascade and parallel realization.

Text Books:

Reference Books:

Unit I

Sampling process: Sampling Theorem, quadrature sampling of Band pass signal, reconstruction of a message from its samples, signal distortion in sampling. Practical aspects of sampling and signal recovery, PAM, TDM.

Unit II

Waveform Coding Techniques: PCM, Channel noise and error probability, quantization noise and SNR, robust quantization. DPCM, DM, ADM, Applications: Digital multiplexers, T1 carrier system. Base-band shaping for Data Transmission: Discrete PAM signals, power spectra of discrete PAM signals, ISI, Ideal solution and Raised Cosine solution.

Unit III

Digital Modulation Techniques: Digital Modulation formats, Coherent binary modulation techniques (ASK, PSK, FSK), Coherent quadrature modulation techniques (minimum shift keying with brief treatment). Non-coherent binary modulation techniques (FSK, DPSK, FSK).

Unit IV


Text Book:

Reference Books:

<table>
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<th>Course Title: Circuit Design with VHDL</th>
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### Unit I

Introduction: VHDL, design flow, EDA tools, translation of VHDL code into circuits, circuit simulation, VHDL syntax, number and character representation in VHDL.


Data types: Introduction, VHDL objects, data-type libraries and packages, Classification of standard data types, logic data types, unsigned and signed data types, fixed and floating point types, predefined data type summary, user defined scalar types, user defined array types, integer Vs enumerated indexing, array slicing, records, subtypes, specifying Port arrays, qualified types and overloading, type conversion, legal Vs illegal assignments, Access types, File types.

### Unit II

Operators & Attributes: Introduction, predefined Operators, overloaded and user-defined operators, predefined attributes, user-defined attributes, synthesis attributes, Group, Alias.


### Unit III

Signals and Variables: Introduction, signal, variable, signal Vs variable, the interference of registers, dual-edge circuits, making multiple signal assignments.

Package and Component: Introduction, Package, Component, Generic Map, Component instantiation with Generate, Configuration, Block.


### Unit IV

Simulation with VHDL Techniques: Introduction, Simulation Types, writing data to files, reading data from files, Graphical simulation (preparing the design), stimulus generation, general VHDL template for testbenches, Type I testbench (manual function simulation), Type II testbench (manual timing simulation), Type III testbench (Automated functional simulation), Type IV testbench (Automated timing simulation), Testbenches with Record types, Testbenches with Data files.

VHDL Design of state machines: Introduction, VHDL template for FSMs, Poor FSM model, FSM encoding Styles, The state-bypass problem in FSMs, systematic Design Technique for timed machines, FSM with repetitive states, Other FSM designs.

### Text Book:


### Reference Books:

<table>
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<tr>
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**Unit I**

System modeling: Definition of control system, Concept of feedback and its significance, open loop and closed loop systems, Modeling of Electrical, Mechanical and Electromechanical systems, Differential equations of physical system. Transfer function, Block diagram representation and Reduction technique, Signal flow graph representation and reduction using Mason’s gain formula.

**Unit II**


**Unit III**


**Unit IV**

Nyquist stability criterion; Principle of argument, mapping, Nyquist path, Nyquist criterion, Nyquist Plot and stability analysis. State Space Analysis;Introduction, concept of state and variables, state model, Non-homogeneous solution of a state equation.

**Text Books:**

1) Nagrath and Gopal: Control System Engineering, New Age published.
**Reference Books:**

<table>
<thead>
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**Unit I**


**Unit II**


**Unit III**


**Unit IV**

Arithmetic contd: Signed, Operand Multiplication, Fast Multiplication, Integer Division, Floating-point Numbers and Operations Basic Processing Unit: Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization, Hard-wired Control and Micro programmed Control

**Text Book:**

Reference Books:

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**Unit I**


**Unit II**


**Unit III**


**Unit IV**


**Text Books:**


**Reference Book:**

1) Jang, Sun and Mizutani, “Neuro-Fuzzy and Soft-Computing – A computational approach to
learning and machine intelligence”, Prentice Hall of India.
Course Title: Pulse and Switching Circuits  
Course Code: UEC517E

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### Unit I

Linear Wave Shaping: The low pass RC circuit, the low pass RC circuit as integrator, the high pass RC circuit, the high pass RC circuit as differentiator, double differentiation, attenuators, RLC circuits, ringing circuits.

### Unit II

Nonlinear Wave Shaping: Clipping Circuits, clamping circuits, Switching Characteristics of Devices: Junction diode switching times, Piece-wise linear diode characteristics, breakdown in junction diodes, Transistor as switch, transistor switching times, breakdown voltages of transistor, the transistor switch in saturation, temperature sensitivity of saturation parameters, design of transistor as switch.

### Unit III

Multivibrators: Bistable multivibrator, a fixed biased bistable mutivibrators, a self biased transistor binary, commutataing capacitors, a non saturating binary, triggering the binary, triggering unsymmetrical through a unilateral devices, triggering symmetrical through a unilateral devices, a direct connected binary, the emitter coupled binary, monostable multivibrator, the collector coupled monostable multivibrator, the emitter coupled monostable multivibrator, the collector coupled astable multivibrator, the emitter coupled astable multivibrator.

### Unit IV

Time Based Generators: General features of time base signal, methods of generating time base waveform, exponential sweep circuits, uni junction transistor, sweep circuit using UJT, sweep circuit using transistor switch, a transistor constant current sweep, Miller and Bootstrap time based generators basic principles, the transistor miller time base generator, the transistor Bootstrap time base generator, current time based generators, a simple current sweep, linearity correction through adjustment of driving waveform, a transistor current time base generator.

Synchronization and Frequency Division: Pulse synchronization of relaxation devices, frequency division in sweep circuits, other astable relaxation circuits, monostable relaxation circuits as dividers, phase delay and phase jitters, synchronization of sweep circuits with symmetrical signals, sine wave frequency division with sweep circuits.

Text Books:
<table>
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<th>Course Title: Random Process</th>
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**Unit I**


**Unit II**


**Unit III**

Pairs of Random variables, Joint CDF, joint PDF, Joint probability mass functions, Conditional Distribution, density and mass functions, EV involving pairs of Random variables, Independent Random variables, Complex Random variables, Engg Application.

**Unit IV**


**Text Book:**

Reference Books:

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### Unit I


### Unit II


### Unit III


### Unit IV

AUTOSAR Standard: Motivation, AUTOSAR Architecture, Main Areas of AUTOSAR Standardization, AUTOSAR Models.

### Text Books:


### Reference Books:


Unit I
Advanced C: Pointers: Concepts, Pointer variables, Accessing variables through pointers, pointer declaration & definition, Initialization of pointer variables, example programs, Pointers and functions, Pointers to Pointers, Compatibility, Lvalue and Rvalue, example programs. Array and Pointers, Pointers arithmetic and array, passing array to a functions, Memory allocation functions, some example programs. Array of Pointers, dynamic array, strings and Pointers, Derived types Enumerated, structure & Union: Type definition, enumerated types, structure, Accessing structures. Complex structures, array of structure, structures and functions, pointers to structures, example programs, unions.

Unit II
Introduction to data structures: Basic concepts, Pseudocode: Algorithm header, Purpose, Conditions and Return, Statement Numbers, Variables, Statement constructs, sequence, selection, loop, Algorithm analysis, Psuedocode example. The abstract data type: Atomic and composite data, Data type, Data structure, Abstract data type, Model for an abstract data type: ADT operations, ADT data structures, ADT Implementations: Array implementation, Linked list implementation, Pointers to linked lists, Generic code for ADTs: Pointer to void, Pointer to Function: Defining pointers to functions, using pointers to functions.
Linear Lists: Stacks: Basic stack operations: Push, Pop, Stack top, Stack linked list: Implementation, Data structure, Stack head, Stack data node, Stack algorithms: Create Stack, Push Stack, Stack top, Empty Stack, Full Stack, Stack count, Destroy Stack.
### Unit III


Queues: Queue Operations: Enqueue, Dequeue, Queue front, Queue rear, Queue example, Queue
Linked list design: Data structure, Queue head, Queue data node. Queue algorithms.

### Unit IV

Queues: Create queue, Enqueue, Dequeue, Retrieving queue data, Empty queue, Full queue, Queue count, Destroy queue, Queue ADT: Queue structure, Queue ADT algorithms, Queue Applications: Categorizing data, Categorizing data design, Categorizing data - C implementation.

General Linear lists: Basic operations, Insertion, Deletion, Retrieval, Traversal, Implementation: Data structure, Head node, Data node, Algorithms, Create list, Insert node, Delete node, List search, Retrieve node, Empty list, Full list, List count, Traverse list, Destroy list, List ADT: ADT functions, Create list, Add node, Internal insertion function, Remove node, Internal delete function, Search list, Internal search function, Retrieve node, Empty list Full list, List count, Traverse, Destroy list.

### Text Books:


### Reference Books:

Course Title: DSP and VHDL Laboratory
Course Code: UEC521L
Credits: 1.5
Contact Hours: 3 Hrs/Week
CIE Marks: 50
SEE Marks: 50
Total Marks: 100

List of Experiments - DSP

Using MATLAB

1) Computation of N point DFT and IDFT
2) Linear and Circular convolution of two sequences using DFT and IDFT.
3) Design and implementation of FIR filter (windowing/frequency sampling method) to meet given specifications.
4) Design and implementation of IIR filter (Chebyshev / Butterworth) to meet given specifications.

Using Digital Signal Processor (TMS 320 C 54XX)

1) Linear and convolution of two given sequences.
2) Computation of N-Point DFT of a given sequence
3) Realization of FIR filter (using any one window) to meet given specifications. The input can be a signal from external source.
4) Realization of a two band graphic equalizer of two different audio bands. The input can be a music signal (music containing different instruments).

List of Experiments - VHDL

1) Write VHDL code using concurrent signal assignment statements for
   a. Full adder
   b. 3:8 decoder with active low output, truth table is shown in table 1.1
   c. 4:1 MUX, truth table is shown in table 1.2
   d. Boolean expressions
      i. F1(abc) = ∑(0,1,3,4,5);
      ii. F2(abc) = π(1,2,3,5,7);
2) Write VHDL code using selected signal assignment statement
   a. Full adder
   b. 3:8 Decoder with active low output truth table shown in table 1.1
   c. 4:1 MUX, truth table is shown in table 1.2
   d. Boolean expressions
      i. F1(abc) = ∑(0,1,3,4,5,);
      ii. F2(abc) = π(1,2,3,5,7);
3) Implementation using conditional signal assignment statement
   a. 8:3 Priority encoder truth table is shown in table 1.3
   b. 3:8 Decoder with active low output truth table shown in table 1.1
c. 4:1 MUX, truth table is shown in table 1.2
d. Boolean expressions
   i. \( F_1(abc) = \sum(0,1,3,4,5,); \)
   ii. \( F_2(abc) = \pi(1,2,3,5,7); \)
4) Write VHDL program using process statement(s) for – combinational circuits
   a. Full subtractor
   b. 2 bit magnitude comparator
   c. 8 bit magnitude comparator
   d. 3:8 decoder
5) Displays
   a. Write VHDL code for BCD to seven segment display decoder
   b. Write VHDL code display following message on LCD
      i. Line 1 : BEC
      ii. Line 2 : ECE
   c. Write VHDL code to run following message from left to right on LCD
      i. Line 1 : BEC
      ii. Line 2 : ECE
   d. Write VHDL code to run following message from right to left on LCD
      i. Line 1 : BEC
      ii. Line 2 : ECE
   e. Write VHDL program to display and blink following message every one second
      i. Line 1 : BEC
      ii. Line 2 : ECE
6) Counters and Shift Register
   a. Write VHDL program for 4-bit up counter and display result on LEDS
   b. Write VHDL program for BCD up counter and display the result on seven segment display
   c. Write VHDL program for 00 to 99 counter and display result on LCD
   d. Write VHDL program for 6-bit SISO shift registers
7) Sequence Detector (1010)
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**List of Experiments**

1) Design and verification of:
   a. Second order active low pass filter
   b. Second order active high pass filter
2) Design and verification of second order band pass filter.
3) Realization of Amplitude modulation and demodulation for a given modulation index.
4) Realization of Frequency modulation.
5) Realization of pulse width modulation.
6) Verification of sampling theorem.
7) Generation and detection of Amplitude shift keying (ASK) Signal.
8) Generation and detection of frequency shift keying (FSK) signal.
9) Generation and detection of phase shift keying (PSK) signal.
10) Study of sample and hold circuit.
11) Realization of pulse Amplitude modulation (PAM)
12) Realization of Pre-emphasis and de-emphasis circuits.
13) Generation of FSK signal using 555 timers.
14) Characterization of Phase Locked Loop (PLL)
15) Generation of PN sequence using shift registers and verification of its properties.